ELEC3607 Embedded Systems

A Simple SDR

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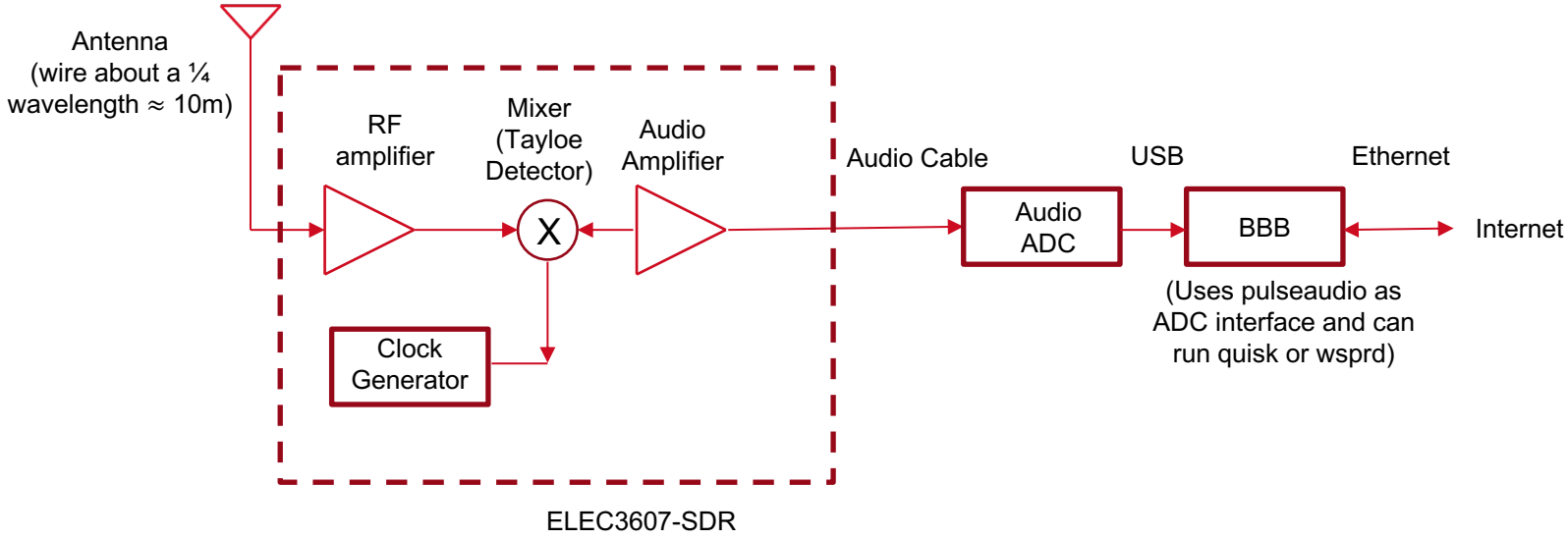
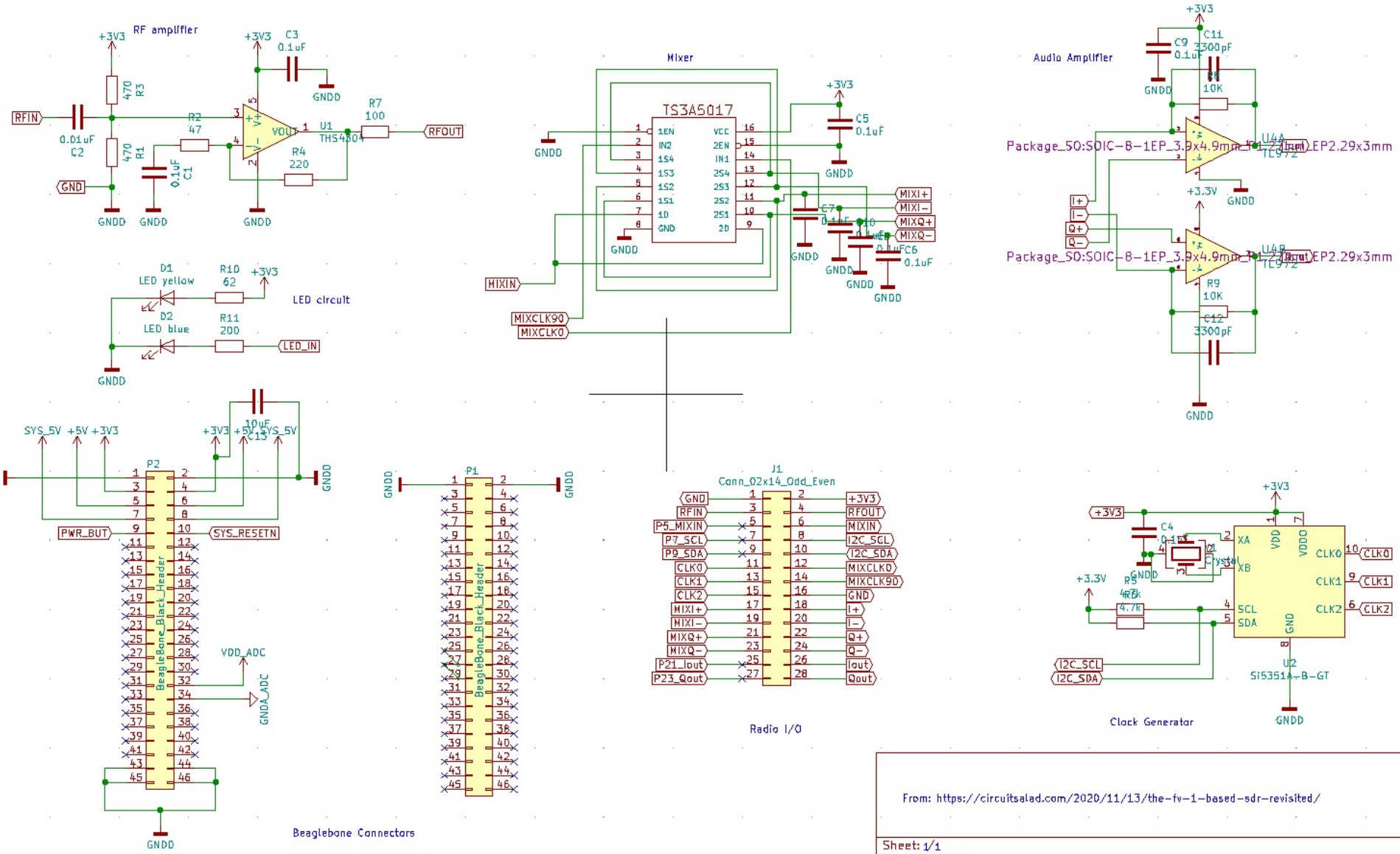
A Simple SDR

- A software-defined radio (SDR) is a radio where components that have been traditionally implemented in analogue hardware (e.g. mixers, filters, amplifiers, modulators/demodulators, detectors, etc.) are instead implemented in software
- In ELEC3607 we are going to construct an SDR receiver (signal of interest is 7.0386 MHz, 200 Hz bandwidth)
- The SDR is designed for simplicity rather than performance
  - A high-performance design would have more filtering, more attention to power supply rejection, etc
  - Circuit comes from https://circuitsalad.com/2020/11/13/
- Note an understanding of the signal processing theory and the electronics are needed to make any system (we focus on the embedded systems aspects)
  - An excellent tutorial on quadrature signals is here https://www.dsprelated.com/showarticle/192.php

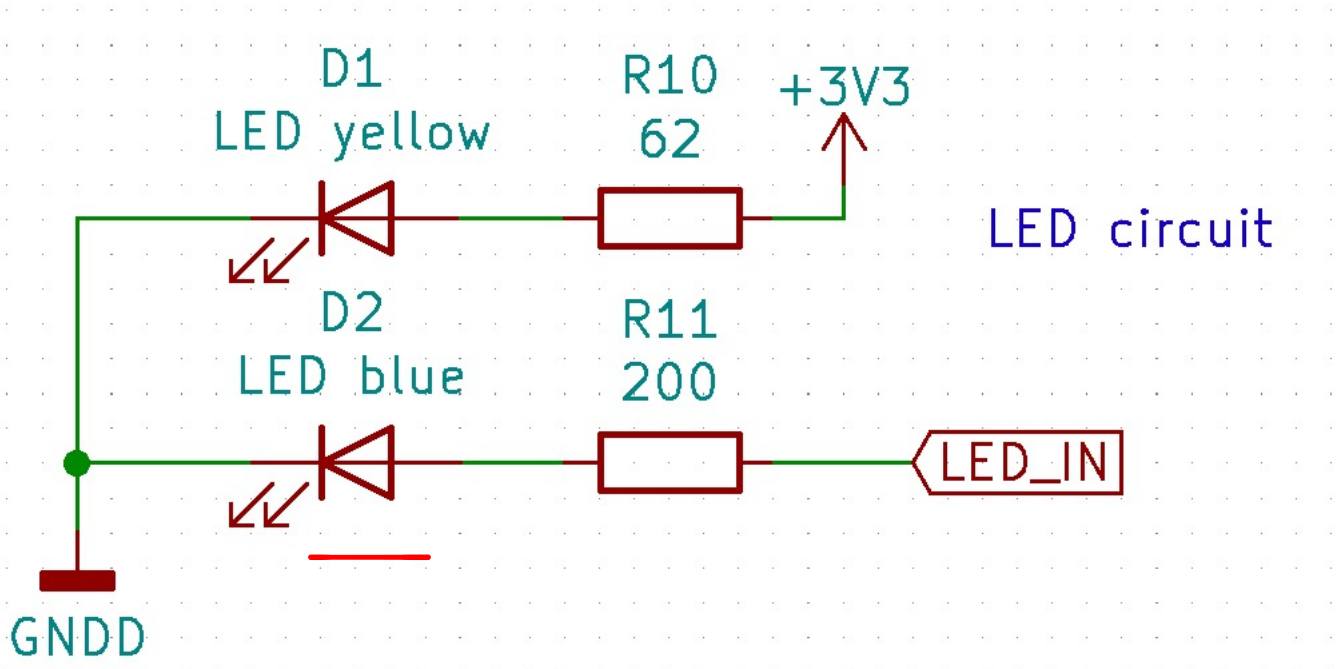
Simplified Block Diagram




RF amplifier
+3V3
C3
0.1uF
GNDD
RFIN
0.01uF
C2
470
R3
R2
47
470
R1
0.1uF
C1
GND
U1
THS4304
R7
100
RFOUT
R4
220
Mixer
TS3A5017
1EN
IN2
1S4
1S3
1S2
1S1
1D
GND
VCC
2EN
IN1
2S4
2S3
2S2
2S1
2D
C5
0.1uF
C7
0.1uF
C6
0.1uF
MIXI+
MIXI−
MIXQ+
MIXQ−
MIXIN
MIXCLK90
MIXCLK0
Audio Amplifier
C9
0.1uF
C11
3300pF
10K
U4A
TL972
Package_SO:SOIC-8-1EP_3.9x4.9mm_P1.27mm_EP2.29x3mm
I+
I−
Q+
Q−
+3.3V
R9
10K
U4B
C12
3300pF
D1
LED yellow
R10
62
D2
LED blue
R11
200
LED circuit
LED_IN
SYS_5V
+5V
10uF
C13
P2
PWR_BUT
SYS_RESETN
BeagleBone_Black_Header
VDD_ADC
GNDA_ADC
Beaglebone Connectors
P1
J1
Conn_02x14_Odd_Even
P5_MIXIN
P7_SCL
P9_SDA
CLK0
CLK1
CLK2
P21_Iout
P23_Qout
I2C_SCL
I2C_SDA
Radio I/O
C4
0.1uF
Crystal
R5
4.7k
R6
4.7k
XA
XB
VDD
VDDO
SCL
SDA
GND
CLK0
CLK1
CLK2
U2
Si5351A-B-GT
Clock Generator
From: https://circuitsalad.com/2020/11/13/the-fv-1-based-sdr-revisited/
Sheet: 1/1
File: bbb.sch
Title: ELEC3607 Software Defined Radio
Size: A4
Date: 4/2/2021
Rev: 0.1
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 1/1

LEDs

Mandatory to have LEDs!



Preamplifier

Simple non-inverting amplifier https://www.ti.com/lit/an/sboa224a/sboa224a.pdf

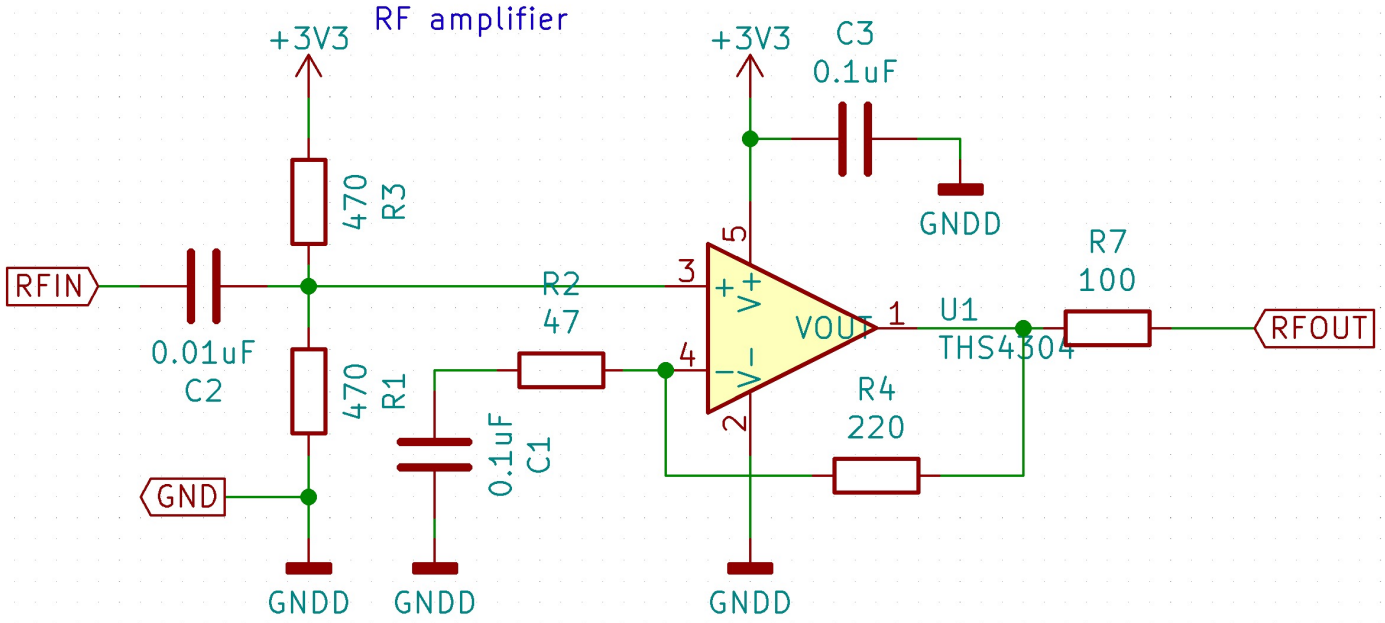
Not a great design (see https://www.analog.com/en/analog-dialogue/articles/avoiding-op-amp-instability-problems.html)

Datasheet: https://www.ti.com/product/THS4304 (low noise, rail-to-rail, high GBW)

High freq gain G=1+R4/R2, low freq gain=1 due to C1

C2 AC couples the input, R1 and R3 make DC level of V+ 3.3V/2

C3 is to bypass the 3.3V supply



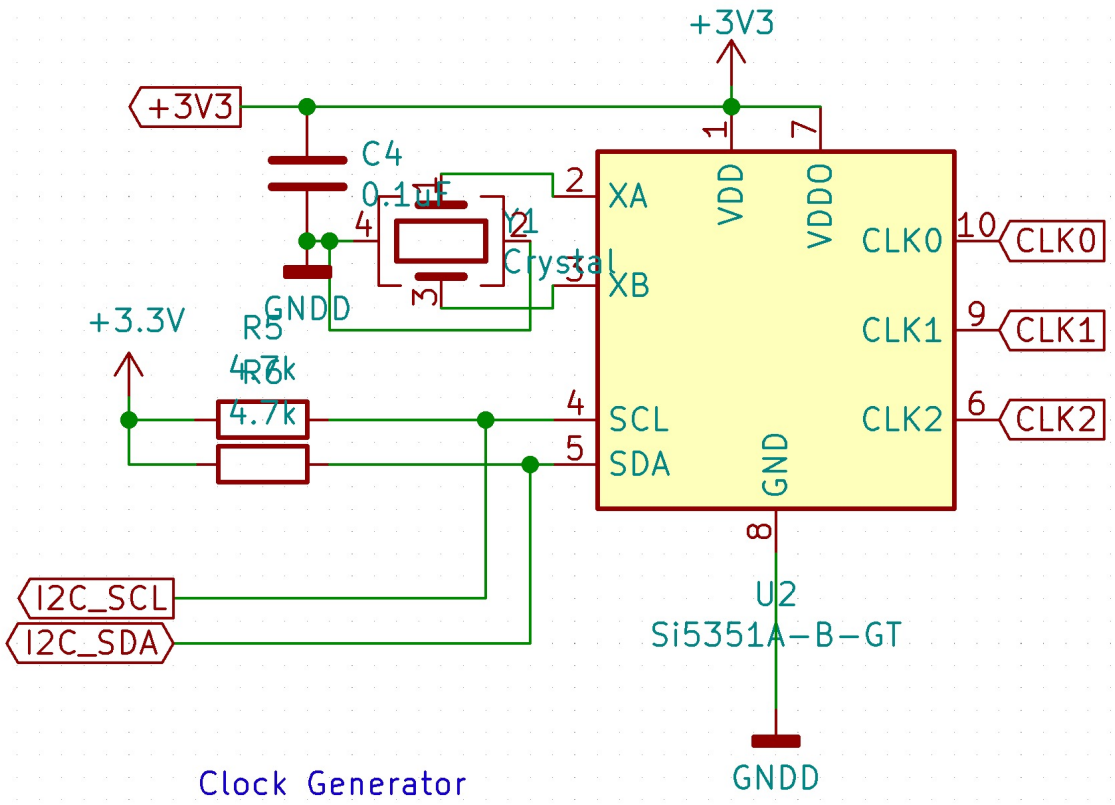
Clock Generator

https://www.silabs.com/timing/clock-generators/cmos/device.si5351a-b-gt

Will program this via BBG to produce two square wave signals CLK0 and CLK1 at appropriate frequency with 90^{o} phase difference

Interface is i2c (discussed later)

C4 is to bypass the 3.3V supply

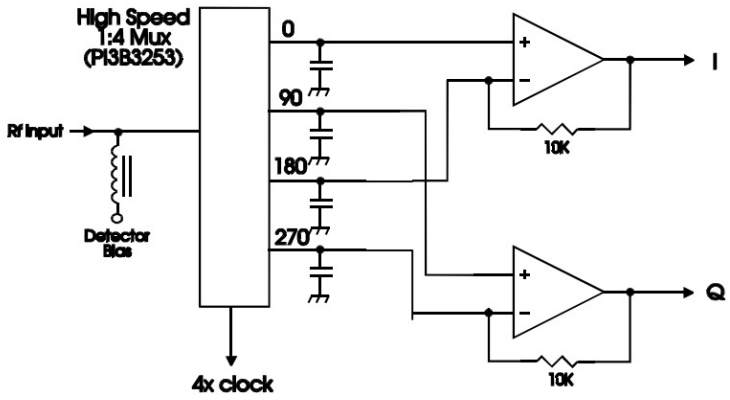


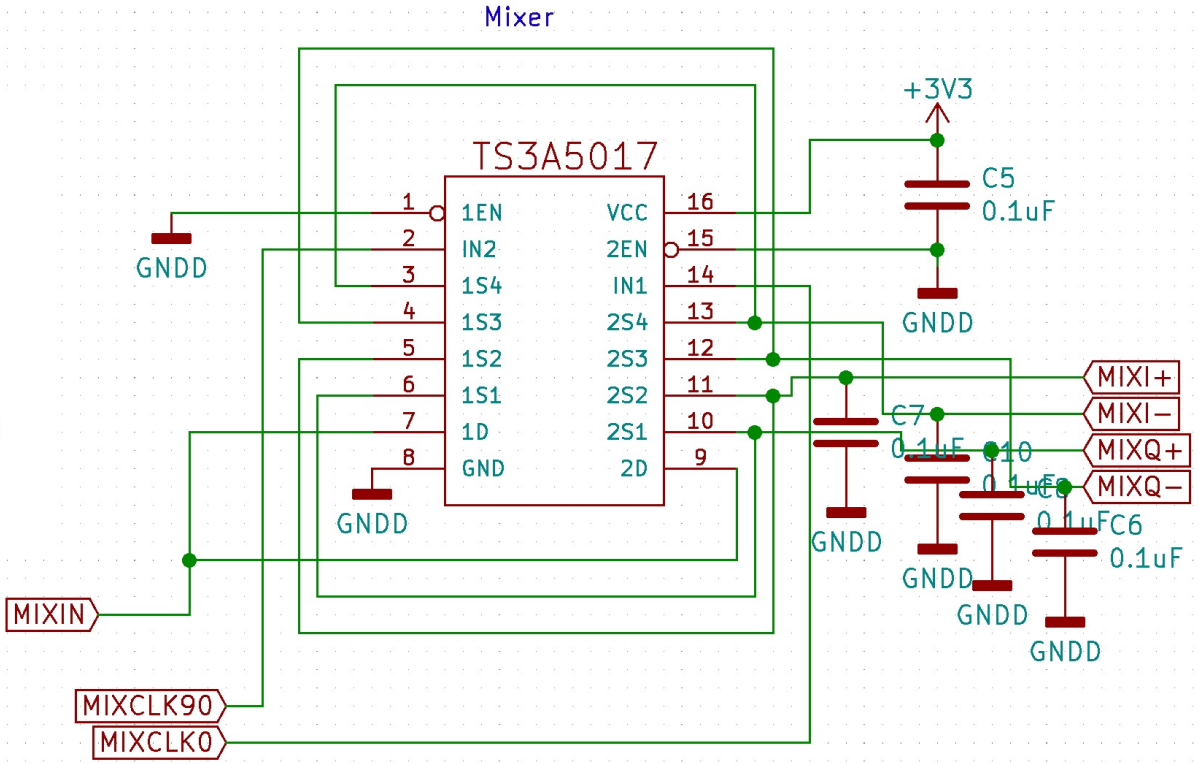
Tayloe Detector

This is a Tayloe detector (http://www.norcalqrp.org/files/Tayloe_mixer_x3a.pdf)

Datasheet https://www.ti.com/lit/ds/symlink/ts3a5017.pdf?ts=1614679120382

C5 is to bypass the 3.3V supply



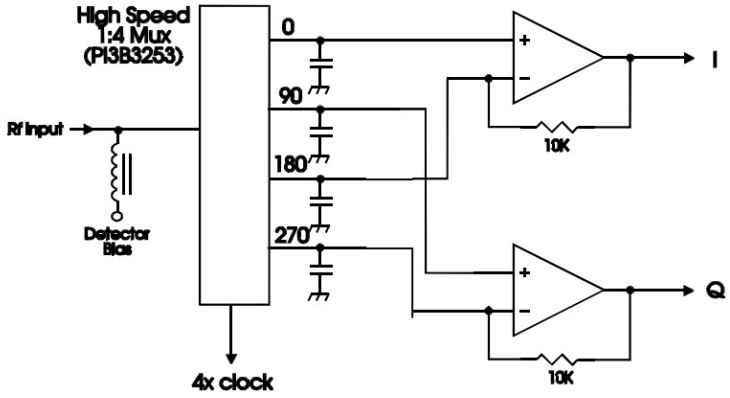


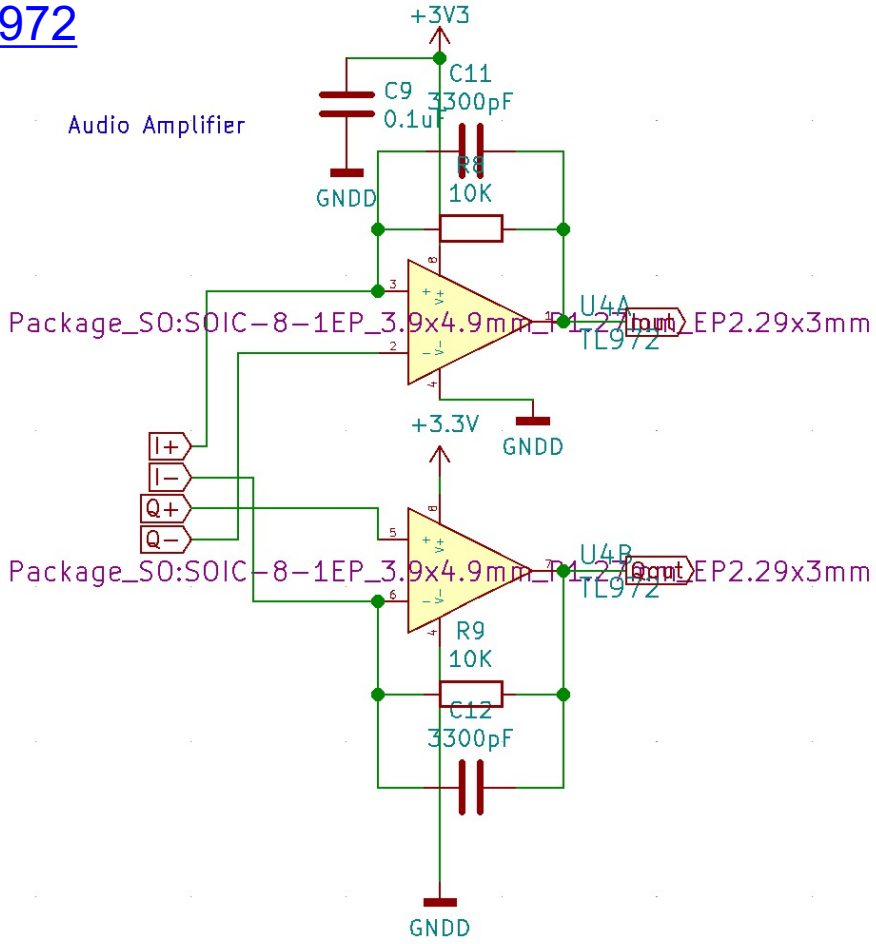
Audio Amplifier

This is an integrator circuit https://www.ti.com/lit/an/sboa275a/sboa275a.pdf

Datasheet https://www.ti.com/product/TL972

C9 is to bypass the 3.3V supply

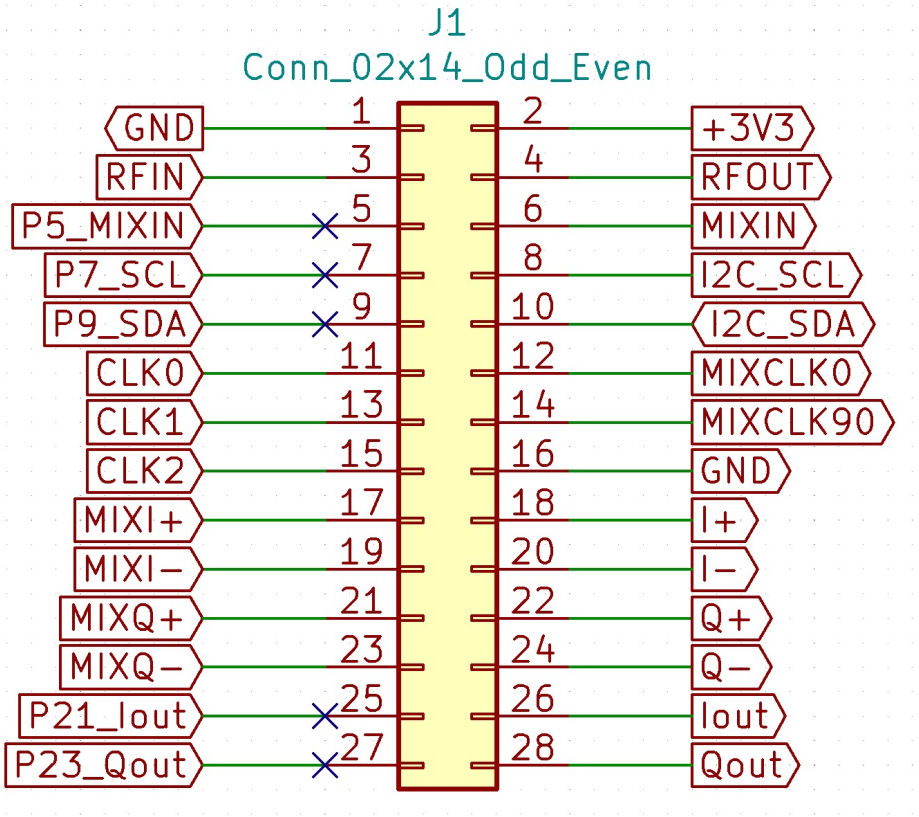




J1 Radio Header

All blocks described are connected to this connector

The BBG will be used to program the Clock Generator and to further process the I/Q output



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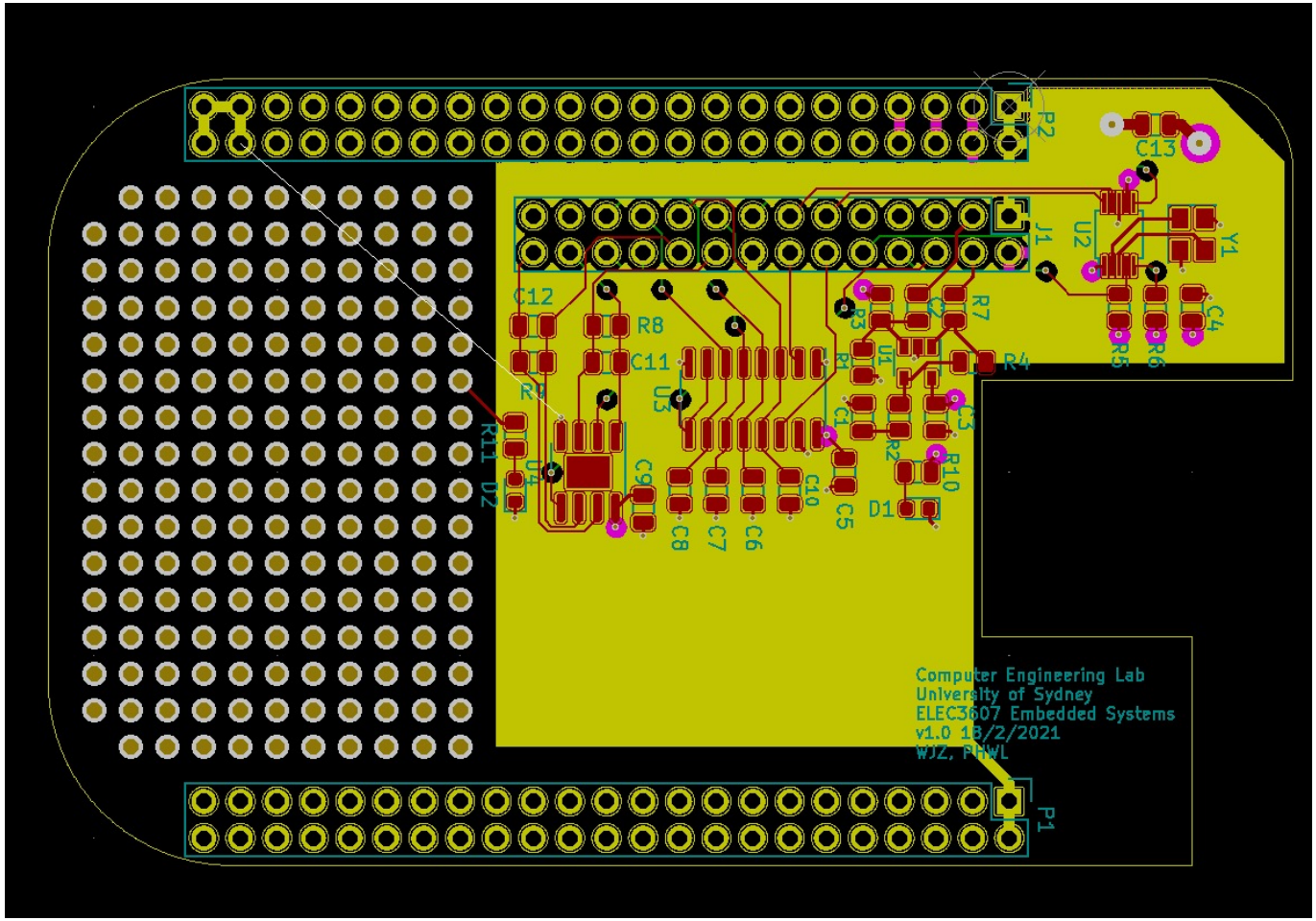
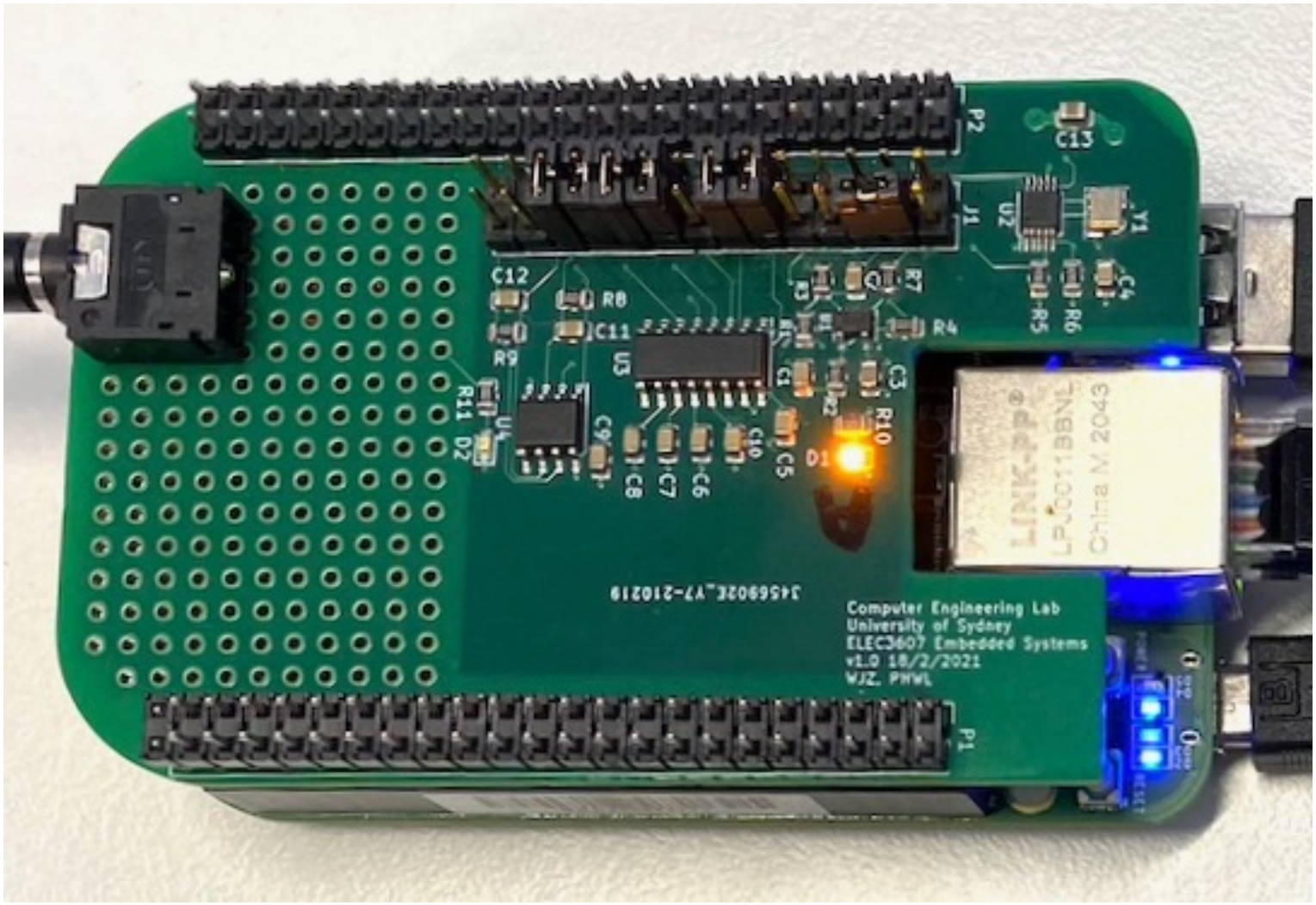
PCB



PCB


P2
C13
J1
U2
Y1
C12
R8
C11
R9
R7
R4
R5
R6
C4
U3
C1
C3
R11
D2
U4
C9
C8
C7
C6
C10
C5
D1
R10
Computer Engineering Lab
University of Sydney
ELEC3607 Embedded Systems
v1.0 18/2/2021
WJZ, PHWL
P1