Energy Filtering Effect at Source Contact on Ultra-Scaled MOSFETs

Johan Saltin, Nguyen Cong Dao, Philip H. W. Leong, *Senior Member, IEEE* and Hiu Yung Wong, *Senior Member, IEEE*

***Abstract*— We postulate that in ultra-scaled Field Effect Transistors (FET), such as nanowires in sub-7nm technology, the source contact will act as an energy filter and increase the effective temperature of carriers arriving at the channel barrier. This is due to the absence of inelastic scattering in the short source-contact-to-channel region. As a result, the Sub-threshold Slope (SS) will increase substantially. In this paper, we verify this energy filtering effect through numerical calculations and Technology Computer-Aided-Design (TCAD) simulations calibrated to quantum solvers for electrostatics. It is found that SS degradation increases as the source metal workfunction increases. At 300K, in the nanowire simulated, SS increases from 94mV/dec to 109mV/dec for gate length, L_G, = 10nm and from 72mV/dec to 88mV/dec for L_G = 15nm, representing an increase of effective carrier temperature from 300K to more than 340K. The simulation result is also verified by including the Schroedinger equation (SE) for tunneling in TCAD simulation. It is also found that such an effect is worse at higher device temperature and disappears at cryogenic temperature.**

***Index Terms*—Sub-threshold Slope, Energy Filter, Nanowire, Schottky Contact, Ballistic Transport**

I. Introduction

One of the main goals in transistor scaling is to increase the drain current ON/OFF ratio (I_{ON}/I_{OFF}) [1] so that the transistor is a close approximation to an ideal switch. There are three ways to achieve this goal. The first is to increase I_{ON} through material engineering, e.g. using high-mobility or strained materials [2]. The second is to reduce I_{OFF} by suppressing leakage, e.g. via Gate-Induced-Drain-Leakage (GIDL) [3]. The third is to reduce the Sub-threshold Slope (SS). This is important especially when the supply voltage is also reduced. The smaller the SS, the more the drain current is reduced as the gate voltage is decreased, and so lower leakage can be achieved for a given I_{ON}. Due to the operating mechanisms in conventional Field Effect Transistors (FET), the minimal SS one can achieve is ln(10)kT/q [4], where k is the Boltzmann Constant, T is the temperature and q is the basic electronic charge. At 300K, this is about 60mV/dec because FET operation is based on the thermionic emission of carriers over a gate-controlled barrier in the channel. SS generally becomes larger (worse) when the transistor is scaled due to the reduction in gate control. Novel transistors based on different mechanisms such as the Tunnel Field Effect Transistor (TFET) [5] and Negative Capacitance FET (NCFET) [6] have been proposed to reduce SS below 60mV/dec at 300K. However, such devices usually either have low I_{ON} or are difficult to optimize.

Therefore, it is expected that traditional FETs will continue to dominate and be scaled to the 1nm technology node for most applications [1][7]. To avoid degradation of SS in ultra-scaled transistors, it is likely that gate-all-around (GAA) structures such as nanowires will be used [1].

It is also well known that Fermi level pinning is inevitable in metal-semiconductor contacts [8]. Therefore, regardless of the metal workfunction, every metal-semiconductor contact is of Schottky type in nature, behaving in an Ohmic manner because of very efficient carrier tunneling through the thin Schottky barrier when the contact is heavily doped [9].

In this paper, we postulate that when a device is sufficiently scaled, due to lack of inelastic scattering in the source region, the source contact can act as an energy filter and increase (worsen) the SS of future ultra-scaled devices. This is confirmed in numerical calculations and then in TCAD simulation of a nanowire (Fig. 1). Therefore, Fermi level de-pinning [10] or source region engineering will be crucial to maintaining low SS in future ultra-scaled devices.

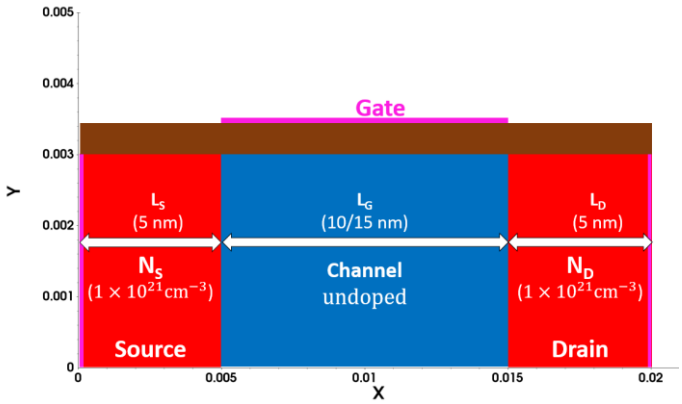

Fig. 1. Half of the cross-section of the nanowire simulated. The nanowire can be constructed by rotating the structure about Y=0μm. The units of the coordinates are in μm. Pink lines represent the electrical contacts. The numbers in the parenthesis are the values used in the simulations.

This paper is based on a paper entitled "Degradation of Sub-Threshold Slope in Ultra-Scaled MOSFETs due to Energy Filtering at Source Contact" presented at the 2019 IEEE S3S Conference.

Manuscript received November 28, 2019.

Johan Saltin and Hiu Yung Wong are with the Electrical Engineering Department, San Jose State University, 1 Washington Sq, San Jose, CA 95192, USA. (*Corresponding author: Hiu Yung Wong*. E-mail: hiuyung.wong@sjsu.edu).

Nguyen Cong Dao and Philip H. W. Leong are with the School of Electrical and Information Engineering, The University of Sydney, Sydney, NSW 2006, Australia.

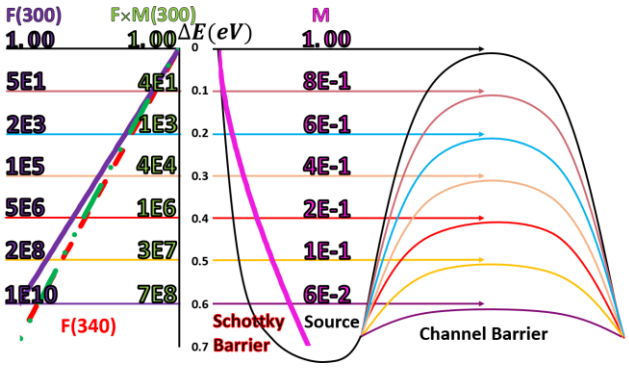

Fig. 2. Illustration of energy filtering effect due to Source Schottky contact. The conduction band diagram is drawn for various surface potentials (from 0V to 0.6V at a step of 0.1V). The 300K electron distribution at metal (f) is plotted in purple. The transmission coefficient (M) of the Schottky barrier is plotted in pink. The carrier distribution after electron tunneling through the Schottky barrier is plotted in green (f×M). f, M and f×M are plotted in log scale and their values at the top of barrier (ΔE=0eV) are normalized to 1. f at T=340K is also plotted for comparison. The values of the functions at 300K are printed at each energy interval. Fermi level is far from the top of the Schottky contact (e.g. at the same level as ΔE=0.6eV) in this calculation to justify the use of Boltzmann statistics.

Some of the results have been reported in 2019 S3S conference [11]. In this paper, we further verify the results by including the Schroedinger equation (SE) for tunneling in TCAD simulation and discuss the validity and limitations of the simulations. The dependency of the energy filtering effect on device temperature from 4K to 400K is also studied.

II. Energy Filtering at Schottky Contact Postulate

Here, an n-type metal/semiconductor (M/S) Schottky contact is used as an example. As shown in Fig. 2, a Schottky contact with a heavily doped semiconductor (e.g. $10^{21}cm^{-3}$) has a thin triangular barrier. Therefore, electrons can tunnel through it very easily in both directions, rendering it Ohmic. At the metal, electrons are thermalized and obey a Fermi-Dirac distribution. In contrast to the common definition of energy, here ΔE is defined as the energy difference between the top of the Schottky barrier (E_{top}) and the energy considered (E) ($\Delta E = E_{top} - E$). Since only the electrons far away (compared to kT) from the Fermi-level are important in this discussion, we approximate the distribution as a Boltzmann distribution, $f \sim e^{\Delta E/kT}$, with the electron density decreasing exponentially as the energy (E) increases (i.e. when ΔE decreases). Since the barrier is thinner at the top, the transmission probability, $M(\Delta E) \sim e^{-3(2mq)^{0.5}\Delta E^{1.5}/4\hbar F}$, derived using WKB approximation, is higher for higher energy electrons. Here, F = 0.5V/nm (which is the typical value obtained in the following TCAD simulations) is used and $m = 0.2m_0$, where m_0 is the rest electron mass. Therefore, right after tunneling from metal to semiconductor, the electron population will no longer follow a Boltzmann Distribution (with more energetic electrons in the total population) and has a higher effective temperature (T_{eff}). T_{eff} can be considered as a parameter to map the new distribution to an equilibrium Boltzmann Distribution. As seen in Fig. 2, T_{eff} is 340K because f(T=300K)×M(T=300K) and f(T=340K) match pretty well overall. This is called the energy filtering effect of a Schottky contact similar to the idea in [12]. In a regular M/S contact, due to phonon scattering, electrons will quickly thermalize to reach thermal equilibrium with the lattice and restore the Boltzmann distribution before reaching the channel barrier, and the regular subthreshold slope based on ln(10)kT/q will still be obtained.

However, if the contact to channel distance is sufficiently short, the electrons will not undergo inelastic scattering with phonons and will reach the channel with higher T_{eff}, increasing SS. This is expected to be true even the source is heavily doped and experiences significant Coulomb scattering, which is an elastic scattering and will not alter the electron distribution in energy space [13].

Reference [14] shows that the mean free path of the electron in silicon nanowire can be as large as 40nm in the <110> direction. According to IRDS [1], the Contacted Poly Pitch is expected to reach 42nm in 5nm technology node, with contact critical dimension (CD) = 14nm and gate length L_G=18nm. Therefore, source contact to channel distance is only (42nm-14nm-18nm)/2=5nm. It is thus expected that electrons tunneling through the source contact (which is Schottky in nature) will arrive at the channel without inelastic scattering and have higher T_{eff} than the device operating temperature.

III. TCAD Simulations

To further verify our theory, TCAD Sentaurus was used to simulate an n-type silicon nanowire [15]. The drift-diffusion carrier transport model (DD) is used to perform the study. DD allows the inclusion of various scattering mechanisms in carrier mobility such as Coulomb scattering due to impurities, surface acoustic phonon and roughness scatterings, and optical phonon scattering (captured in high field saturation model). These models are included by activating Masetti Model, Lombardi Model and Extended Canali Model in the simulation [15]. The carrier transport in nanowire is assumed to be in the <100> direction. The density gradient model for electrons is used to account for quantum confinement effects (except simulations in Fig. 6, 7 and 8 where convergence is difficult due simulation at cryogenic temperature or inclusion of Schroedinger equation) and is calibrated against a Non-Equilibrium Green's Function (NEGF) transport model [16]. Self-heating is not included for simplicity and better convergence. The gate workfunction is set to 4.6eV. A Schottky boundary condition is used for the source contact with various metal workfunctions. The non-local tunneling model using WKB approximation is used to model the tunneling of electrons into the nanowire from the contacts with tunneling mass = $0.2m_0$. Fig. 1 shows the structure simulated.

The non-local tunneling model is set up to have two options [17][15]. One is to have the electrons tunneled from the metal thermalized immediately after the Schottky barrier. This represents the case when there is no energy filter effect as all tunneled carriers are thermalized before reaching the channel. Another option is to send the tunneled electron to the top of the channel barrier after Schottky barrier tunneling, which is equivalent to ballistic transport from the Schottky Source to

the top of the channel barrier. This represents the case when there is no inelastic scattering and the electrons reach the channel barrier at a higher temperature (Fig. 2 and Fig. 3)

IV. Simulation Results

Figure 3 shows that when the source metal workfunction is 5.1eV, the subthreshold slope (using the slope from I_D = 10^{-10}A to 10^{-8}A) is degraded from 94mV/dec to 109mV/dec for L_G=10nm as predicted. This is equivalent to T_{eff} = 347K using $SS = n \ln 10 \frac{kT}{q}$, where n is the non-ideality factor. By assuming the ballistic transport and non-ballistic transport cases have the same *n* and since the non-ballistic case has device temperature equals to the ambient temperature (300K in this case), T_{eff} is found by considering the ratio of SS of both cases. This is similar to the numerical calculation. It also shows the conduction band profile from source to drain when the transport in the source is treated ballistically. As the gate voltage increases, the channel barrier reduces, and more electrons can go over the barrier. However, due to the energy filtering effect at the source contact, the number of extra electrons that can overcome the barrier when the channel barrier is lowered, less than when the distribution was Boltzmann. As a result, it has a large SS.

Figure 4 shows the change of SS as a function of the source metal workfunction (WF) for L_G=10nm and 15nm. The SS degradation starts when WF is at 4.4eV and becomes worst when WF = 5.1eV. When WF is 4.3eV or less, in the off state, the channel barrier is higher than the Schottky barrier and the transmission coefficient is 100% (quantum reflection is ignored) and there is no energy filtering effect. As a result, there is no SS degradation when the WF is low.

V. Temperature Effect

The effect of energy filtering at source contact is expected to have strong temperature dependency because the effect is a result of the deviation of the carrier distribution in the energy space from equilibrium Boltzmann and Fermi-Dirac distributions. Transistors usually operate at elevated temperatures due to self-heating, especially in high-performance CPUs and GPUs. Therefore, it is important to understand how energy filtering effect changes at elevated temperatures. Nowadays, there is also an increased interest in the cryogenic applications of CMOS circuits as quantum

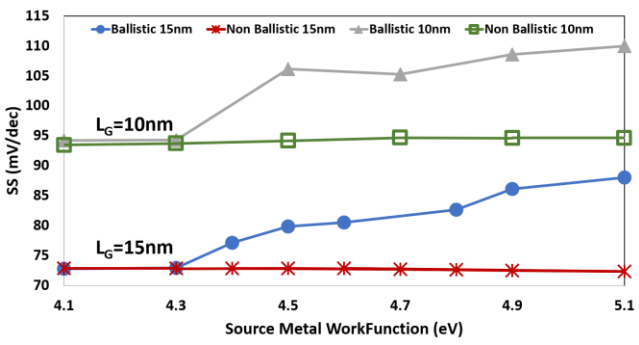

Fig. 4. SS of nanowires as a function of source metal Workfunction.

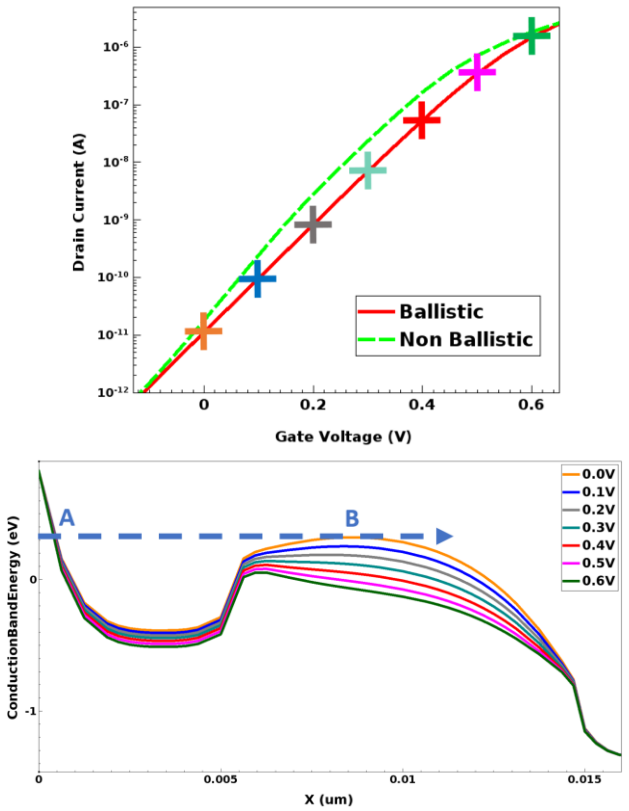

Fig. 3. The subthreshold region of the I_D-V_G of the nanowire with L_G=10nm with source metal WF=5.1eV (top). The corresponding conduction band profiles from source to drain are shown at the bottom. One of the tunneling paths is illustrated. In the non-ballistic case, electrons are thermalized at "A" once passing through the Schottky barrier. In ballistic case, electrons are not allowed to thermalized until they have passed the peak "B" of the channel barrier.

computer peripheries. Cryogenic CMOS shows abnormal SS when the device temperature is less than 30K [18][19]. For example, at 4.2K, the SS is ~11mV/dec instead of the theoretical value of 0.8mV/dec. However, there is no consensus on the root cause of such abnormal behavior [20]. Therefore, it is also important to understand if such behavior can be a result of source contact energy filtering because at cryogenic temperature, the inelastic scattering rate reduces

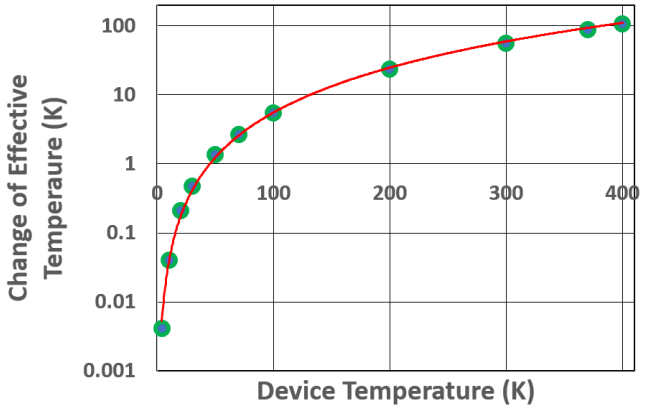

Fig. 5. Calculated change of T_{eff} as a function of device temperature. Markers are results from calculation and red line is a power law fitting curve. source metal workfunction = 5.1eV is assumed.

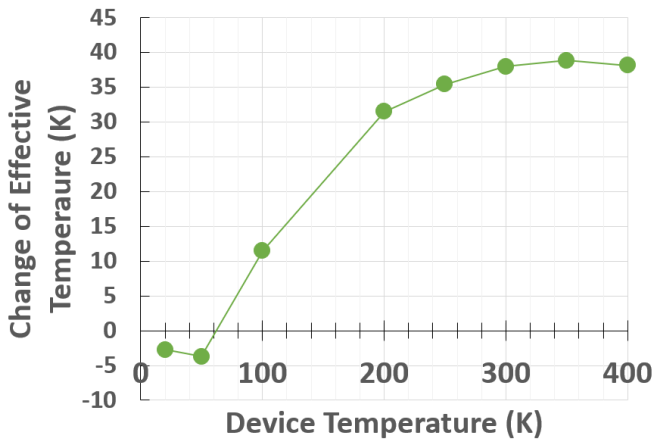

Fig. 6. TCAD simulated changes of T_{eff} as a function of device temperature. L_G = 10nm and source metal workfunction = 5.1eV are used. V_D = 0.1V. Quantum correction is turned off.

substantially due to lack of phonon scatterings. It is possible such an energy filtering effect exists in larger transistors due to the much longer mean free path for ballistic transport.

By using the methodology illustrated in Fig. 2, T_{eff} in the subthreshold region is calculated for the device with source metal WF = 5.1eV from 4K to 400K. Fig. 5 shows that the change of T_{eff} increases with device temperature. This is because at higher temperatures, electron distribution in energy space is broadened and this increases the effect of energy filtering. On the other hand, at lower temperatures, the change of T_{eff} reduces and approaches zero at 0K. This is because the energies of the electrons participating in the tunneling in the subthreshold region concentrate in a very narrow band around the Fermi level and will not "feel" the different transmission coefficients at different energies as much. It can also be better understood by considering in the extreme case when T = 0K, only the electron at the Fermi level will participate in the conduction when the transistor switches from off-state to on-state, and thus, the shape of the source Schottky barrier does not have any effect in altering the electron distribution after tunneling.

To verify the calculation, TCAD simulation is also performed for the device in Fig. 1 with L_G = 10nm from 20K to 400K as showed in Fig. 6. Since convergence is known to be challenging at sub-100K TCAD simulation, V_D is set to 0.1V and quantum correction is turned off in the simulations in Fig. 6 and Fig. 7. It is found that TCAD simulation gives a similar trend as the calculation in Fig. 5. The major difference is, at 400K, the change of T_{eff} is not as much as in calculation. This is because thermionic emission over the source Schottky barrier becomes more important at higher temperatures while thermionic emission contribution to the transport is neglected in the calculation. This reduces the effect of the filtering effect due to tunneling. At device temperature less than 50K, the ballistic case has smaller T_{eff} than the non-ballistic case but only by about 3K. This is due to the noise in the simulation, such as the non-straight curve in the sub-threshold region of the 20K case (Fig. 7). Based on the calculation and simulation results, therefore, the energy filtering effect at source contact cannot cause the abnormal SS in cryogenic CMOS.

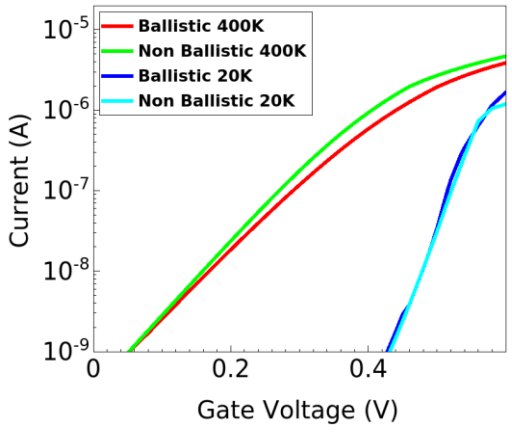

Fig. 7. I_D-V_G curves obtained from TCAD simulations at 400K and 20K for ballistic and non-ballistic cases. L_G = 10nm and source metal workfunction = 5.1eV are used. V_D = 0.1V. Quantum correction is turned off.

VI. Discussion

One of the major assumptions in this study is that the electrons will retain the distribution of f(T=300K) × M(T=300K) in the source region due to the lack of inelastic phonon scattering. However, electron-electron scattering is not considered, which redistributes the energy and momentum among the electrons [21]. Due to the high electron concentration at the source, the relaxation time is about 0.1fs [22]. Therefore, the electrons are in equilibrium with each other but still at an elevated effective temperature as a whole when they reach the channel barrier. As a result, it is expected that in the ballistic case, the SS slope may be different from what has been calculated but still worse than the non-ballistic case.

As pointed out in [23], the metal-semiconductor interface is one of the most challenging problems in solid-state physics. It is expected rigorous self-consistent quantum transport simulation is needed for quantitatively correct results, in order to account for e.g. source starvation [24], sub-band formation and image force. However, since both ballistic and non-ballistic cases share the same setup, it is expected that our result is still qualitatively correct.

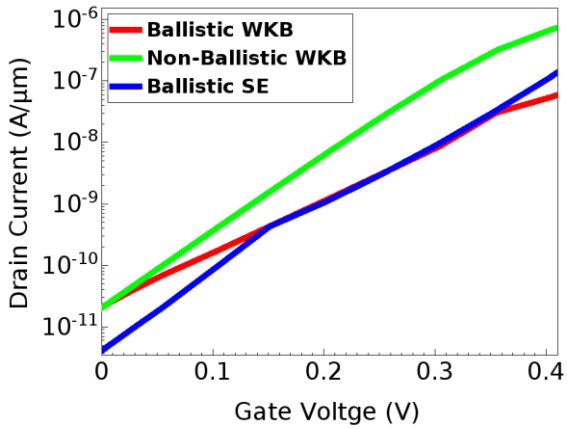

Fig. 8. I_D-V_G curves of L_G=10nm with V_D=0.01V with source WF=5.1eV. Density gradient and high field saturation models were not turned on for better convergence. Blue is shifted vertically for easy comparison.

This study doesn't take the backscattering of electrons from the channel barrier into account, which can reduce the ballisticity [25][26]. However, as shown in [25], backscattered carriers are only a small portion of the carriers even at 15nm and it is expected to be less at 10nm or below. Therefore, most of the carriers are still expected to transport ballistically.

In the extreme case of WF=5.1eV and doping of $10^{21}cm^{-3}$, the depletion width is only 1.5nm and comparable to the de Broglie wavelength of the electrons. Error in WKB approximation may become large theoretically. It is desirable to solve the Schroedinger equation (SE) for M. However, convergence is difficult in TCAD when SE is included. By using a reduced model setup (no quantum correction and high-field saturation model is turned off) and a low drain bias (V_D = 0.01V) for better convergence, it is confirmed that WKB gives a similar result as in SE (Fig. 8). Therefore, WKB still gives qualitatively correct results despite the possible error in the approximation.

This results in this study applies not only to MOSFET but also to other transistors such as Schottky-Barrier (SB) Transistor using Si or 2D materials [27]. Since the source in SB transistor are undoped and thus lack of elastic Coulomb scatterings due to ionized dopants, it is expected that the energy filtering effect will be more prominent.

VII. Conclusion

We report that in ultra-scaled FET, SS will be larger than expected due to the energy filtering effect in the source contact. This is because every source contact is Schottky in nature and if there is a lack of inelastic scattering in the source region, carriers cannot thermalize with the lattice before they reach the channel. Numerical calculation and TCAD simulation show that T_{eff} increases from 300K to more than 340K. The result is also validated by solving the Schroedinger equation (SE) for M in TCAD simulation. Therefore, it is important to either avoid Schottky contact at the source (e.g. through Fermi-Level de-pinning engineering [10]) or special source region engineering is required. Moreover, it is also found that such an energy filtering effect becomes worse at higher temperatures and disappears at cryogenic temperatures. Therefore, such energy filtering effect is not the cause of the abnormal SS in cryogenic CMOS.

Acknowledgment

The authors thank Synopsys Inc. for the donation of TCAD licenses and Dr. Andreas Wettstein of Synopsys for his fruitful discussion and advice on the use of non-local tunneling model. H. Y. Wong thanks the support from San Jose State University College of Engineering's new faculty start-up fund.

References

[1] (2017). International Roadmap for Devices and Systems – More Moore. [Online]. Available: https://irds.ieee.org/images/files/pdf/2017/2017IRDS_MM.pdf

[2] F. Conzatti, N. Serra, D. Esseni, M. D. Michielis, A. Paussa, P. Palestri, L. Selmi, S. M. Thomas, T. E. Whall, D. Leadley, E. H. C. Parker, L. Witters, M. J. Hÿtch, E. Snoeck, T. J. Wang, W. C. Lee, G. Doornbos, G. Vellianitis, M. J. H. van Dal, and R. J. P. Lander, "Investigation of Strain Engineering in FinFETs Comprising Experimental Analysis and Numerical Simulations," in IEEE Transactions on Electron Devices, vol. 58, no. 6, pp. 1583-1593, June 2011. doi: 10.1109/TED.2011.2119320

[3] P. Kerber, Q. Zhang, S. Koswatta and A. Bryant, "GIDL in Doped and Undoped FinFET Devices for Low-Leakage Applications," in IEEE Electron Device Letters, vol. 34, no. 1, pp. 6-8, Jan. 2013. doi: 10.1109/LED.2012.2224089

[4] S. M. Sze, *Physics of Semiconductor Devices.* John Wiley & Sons, 1981, ch. 6.

[5] A.M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," Nature, 479 (7373) (2011), pp. 329-337. doi: 10.1038/nature10679.

[6] S. Salahuddin and and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," Nano Letters, vol. 8, no. 2, pp. 405–410, 2008. doi: 10.1021/nl071804g.

[7] J. Fang, W. G. Vandenberghe, B. Fu, and M. V. Fischetti, "Pseudopotential-based electron quantum transport: Theoretical formulation and application to nanometer-scale silicon nanowire transistors", Journal of Applied Physics 119 (3), 035701.

[8] V. Heine, "Thoery of Surface States", Phys. Rev.138, A1689 (1965). doi: 10.1103/PhysRev.138.A1689

[9] Dieter K. Schroder, Semiconductor Material and Device Characterization. 2nd ed. New York: Wiley, 1998, pp. 133-138. doi: 10.1002/0471749095

[10] Raisul Islam, Gautam Shine, and Krishna C. Saraswat, "Schottky barrier height reduction for holes by Fermi level depinning using metal/nickel oxide/silicon contacts", Appl. Phys. Lett. 105, 182103 (2014); doi: 10.1063/1.4901193

[11] J. Saltin, N. C. Dao, P. H. W. Leong, and H. Y. Wong, "Degradation of Sub-Threshold Slope in Ultra-Scaled MOSFETs due to Energy Filtering at Source Contact," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, San Jose, CA, 2019.

[12] E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi and G. Baccarani, "Investigation on superlattice heterostructures for steep-slope nanowire FETs," 69th Device Research Conference, Santa Barbara, CA, 2011, pp. 201-202. doi: 10.1109/DRC.2011.5994497

[13] David Esseni, Nanoscale MOS Transistors: Semi-Classical Transport and Applications. 2nd ed. Cambridge University Press, 2011, pp.130-205. doi: 10.1017/CBO9780511973857

[14] M. P. Persson, A. Lherbier, Y.-M. Niquet, F. Triozon, and S. Roche, "Orientational dependence of charge transport in disordered silicon nanowires," Nano Lett., vol. 8, no. 12, pp. 4146–4150, Nov. 2008. doi: 10.1021/nl801128f.

[15] Sentaurus™ Device User Guide Version O-2018.06, June 2018.

[16] H. Y. Wong, N. Braga and R. V. Mickevicius, "Enhancement-Mode Recessed Gate and Cascode Gate Junctionless Nanowire With Low-Leakage and High-Drive Current," in IEEE Transactions on Electron Devices, vol. 65, no. 9, pp. 4004-4008, Sept. 2018. doi: 10.1109/TED.2018.2856740

[17] MeiKei Ieong, P. M. Solomon, S. E. Laux, H.-P. Wong and D. Chidambarrao, "Comparison of raised and Schottky source/drain MOSFETs using a novel tunneling contact model," International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217), San Francisco, CA, USA, 1998, pp. 733-736. doi: 10.1109/IEDM.1998.746461

[18] A. Beckers, F. Jazaeri and C. Enz, "Characterization and Modeling of 28-nm Bulk CMOS Technology Down to 4.2 K," in IEEE Journal of the Electron Devices Society, vol. 6, pp. 1007-1018, 2018. doi: 10.1109/JEDS.2018.2817458

[19] Avid Kamgar, "Subthreshold behavior of silicon MOSFETs at 4.2 K," Solid-State Electronics, Volume 25, Issue 7, July 1982, Pages 537-539. doi: 10.1016/0038-1101(82)90052-1

[20] Arnout Beckers, Farzan Jazaeri, and Christian Enz, "Revised theoretical limit of the subthreshold swing in field-effect transistors," July 2019, arXiv:1811.09146v2.

[21] A. Schenk, Advanced Physical Models for Silicon Device Simulation. 1st ed. Wien: Springer-Verlag, 1998, pp. 34. doi: 10.1007/978-3-7091-6494-5

[22] B. K. Ridley, Quantum Process in Semiconductor. 5th ed. United Kingdom: Oxford University Press, 2014, pp. 150. doi: 10.1080/00107514.2014.933258

[23] A. Schenk, "1D analytical model of the metal-semiconductor contact beyond the WKB approximation," Solid State Electronics, Volume 37, Issue 9, p. 1633-1647. doi: 10.1016/0038-1101(94)90046-9

[24] M. V. Fischetti, L. Wang, B. Yu, C. Sachs, P. M. Asbeck, Y. Taur and M. Rodwell, "Simulation of Electron Transport in High-Mobility

MOSFETs: Density of States Bottleneck and Source Starvation," 2007 IEEE International Electron Devices Meeting, Washington, DC, 2007, pp. 109-112. doi: 10.1109/IEDM.2007.4418876

[25] N. Sano, "Kinetics of Quasiballistic Transport in Nanoscale Semiconductor Structures: Is the Ballistic Limit Attainable at Room Temperature?," Physical Review Letters, 93, 246803 (2004).

[26] M. V. Fischetti, S. Jin, T.-W. Tang, P. Asbeck, Y. Taur, S. E. Laux, M. Rodwell and N. Sano, "Scaling MOSFETs to 10 nm: Coulomb effects, source starvation, and virtual source model, J Comput Electron (2009) 8: 60–77.

[27] A. Prakash, H. Ilatikhameneh, P. Wu and J. Appenzeller, "Understanding contact gating in Schottky barrier transistors from 2D channels," Sci Rep 7, 12596 (2017). https://doi.org/10.1038/s41598-017-12816-3.